REMARKS

This amendment is being filed in response to the Office Action having a mailing date of July 13, 2005. Claims 1 and 18 are amended. New claims 19-20 are added. No new matter has been added. With this amendment, claims 1-20 are pending in the application.

In the Office Action, claims 1-18 were rejected under 35 U.S.C. § 102(a) as being anticipated by Perner (U.S. Patent No. 6,501,697). For the reasons set forth below, the applicants respectfully request the Examiner to reconsider and to allow the pending claims.

I. Discussion of the Applicant's Disclosed Embodiments

A disclosed embodiment will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiment, and the discussion of the differences between the disclosed embodiment and subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences are intended to merely help the Examiner appreciate important claim distinctions discussed thereafter.

One embodiment of the present invention relates to a sense amplifier (SA2) for reading a memory cell, comprising a read node (RND) linked directly or indirectly to the memory cell, a first active branch connected to the read node (RND). The first active branch comprises a means (TP3, TN3) for supplying a read current at the read node, and a data output (SOUT) linked to one node of the first active branch at which a voltage (VMID1) representative of the conductivity state of the memory cell appears. An embodiment of the sense amplifier comprises a second active branch connected to the read node, with the second active branch comprising means (TP5, TN4) for supplying, at the read node, a current (Iref2) that is added to the current (Iref1) supplied by the first active branch, such that the voltage (VMID1) representative of the conductivity state of the memory cell remains substantially stable upon a current draw at the read node. *See, e.g.*, Figure 3 and the accompanying description in the present application.

II. Discussion of Perner in View of the Applicant's Disclosed Embodiments

In the Office Action, the Examiner has taken the position that Perner (Figure 4 and column 6, lines 1+) discloses the first active branch that supplies the read current at the read node and the second active branch that supplies a current that is added to the current supplied by the first active branch. The applicant respectfully disagrees with this interpretation of Perner.

The sense amplifier 38 shown in Figure 4 and described col. 6 and 7 of Perner comprises a sense side (left side) and a reference side (right side), which are different than the first and second active branches disclosed by the applicants in the present application.

A. The sense side of Perner

The sense side of Perner has a sense node 70 connected to a memory element represented by a resistor R_M and a diode 62 (representing the nonlinear part of the memory element). The voltage Vs′ of the sense node is maintained at the vicinity of an external voltage Vs by a pull-down transistor Q1, the gate of which is driven by an operational amplifier A1, which receives the sense node voltage Vs′ and the external voltage Vs. Non-selected memory elements are schematized by a resistor Rp and a diode 68 connected to the sense node 70 and biased by the external voltage Vs.

The operational amplifier A1 supplies a gate control voltage to transistor Q1 to have the sense node voltage Vs′ equal or close to external voltage Vs. The gate control voltage supplied by operational amplifier A1 is the image of the current flowing through the memory element, and is translated by a mirroring effect, through a translator transistor Q2, to a first input of a comparator 76.

B. The reference side of Perner

The reference side of Perner has the same structure as the sense stage but is designed to sense two emulated memory elements that are emulated by reference resistors R_H and R_L and their associated diodes 64, 66, with resistance R_L emulating a memory element in the high resistance state and resistance R_H emulating a memory element in the low resistance state.

The non-selected memory elements are also emulated by a resistor Rp/2 and an associated diode 69.

The voltage Vss′′ at node 72, called reference voltage, is the sense voltage of the emulating resistors R_H and R_L. The node 72 is the equivalent of a sense node for sensing emulated memory elements. Reference voltage Vss′′ is also regulated at the vicinity of voltage Vs by a feed-back operational amplifier A2 and a pull-down transistor Q3, the gate of which is driven by the operational amplifier A2. As in the sense side, the gate control voltage supplied by operational amplifier A2, is the image of the current flowing through the emulating resistors R_H, R_L and is translated to a second input of comparator 76 through a current mirroring arrangement comprising a translator transistor Q4.

C. Supplying a read current at the read node (first branch)

Perner's sense amplifier does not disclose, teach or suggest a first active branch that includes a "means for supplying a read current at the read node." In Figures 1, 3 or 5 of the present application, an example means for supplying a read current at the read node comprises a pull-up transistor TP3 that imposes current Iref at the read node RND by mirroring effect, Iref being a function of the current Ibias. As explained above, Perner's sense amplifier only comprises the pull-down transistor Q1 to control voltage Vs′ at node 70.

The problem that one embodiment of the applicant's invention solves is directly linked to the fact that the sense amplifier supplies the read current. This technical problem can be understood in relation with the admitted prior art of Figure 1 of the present application:

> When a voltage drop C1 occurs in the supply voltage Vcc, stray capacitances absorb the variations of the voltage Vref and the difference between the voltages Vref and Vcc decreases and becomes lower than the threshold voltage of the transistors TP1, TP3, which go off. As the transistor TP1 is off, the voltage VC1 drops and the transistor TN3 also goes off. The low current passing through the memory cell MCELL starts to discharge the bit line. Then, when a peak P1 occurs on the voltage Vcc, the difference between the voltages Vref and Vcc increases and the transistors TP1, TP3 rapidly become on. The voltage VC1 increases and exceeds the value it had before the occurrence of the

voltage drop. The transistor TN3 becomes on. If the current Icell required by the bit line is higher than the current Iref supplied by the transistor TP3, the voltage VMID1 drops as represented in Figure 2. As a result, the output of the inverting gate temporarily goes to 1. If the latch DL latches the datum at this instant, the result of the read is false.

In contract, this problem does not seem to concern the sense amplifier of Perner. In Perner's sense amplifier, the sense node 70 and the reference node 72 do not supply the sensing current and the reference current, and only regulate the sense voltage Vs′ and the reference voltage Vs′′ at the vicinity of Vs, by means of operational amplifier A1 and pull-down transistor Q1 and operational amplifier A2 and pull-down transistor Q3, respectively.

Thus, if a drop or a peak appears in the read voltage V_R, both sense voltage Vs′ and reference voltage Vs′′ of Perner remain controlled at the vicinity of Vs′ thanks to operational amplifiers A1, A2 and transistors Q1, Q3. Even if the peak or drop of voltage V_R cause a peak or a drop in the two translated gate control voltages output by operational amplifiers A1, A2, the respective drops or peaks should have similar shapes due to the symmetrical architecture of the sense amplifier and these symmetrical variations should not be detected by the differential amplifier 76.

Therefore, Perner's sense amplifier only comprises means for controlling the voltage at the pull-down read node 70 and deducing the current flowing through the memory element by translating the gate control voltage output by operation amplifier A1 at the input of differential amplifier 76. Perner's sense amplifier does not supply a read current at the read node.

D. Supplying a current added to the current supplied by the first branch

The Examiner also asserts that Perner's sense amplifier has a second active branch connected to the read node, comprising means for supplying, at the read node, a current that is added to the current supplied by the first active branch, such that the voltage representative of the conductivity state of the memory cell remains substantially stable upon a current draw at the read node. To that purpose, the Examiner simply refers to "col. 6 lines 1+" of

Perner, that is, the description of the sense circuitry of Figure 4. This reference is vague and does not prove anything, however.

Assuming that the Examiner has taken the position that the reference side (right side) of the sense amplifier of Perner, which sense emulated memory elements R_H, R_L, is the "second active branch" connected to the read node, it is obvious that this reference side is not connected to the read/sense node 70. Moreover, the reference current sensed by the reference side is not added to the current flowing through the memory element R_M + diode 62 and is simply compared to this current by the comparator 76.

Assuming that the Examiner has taken the position that operational amplifier A1 as well as transistor Q1 of Perner form the applicants' disclosed "second active branch," the amplifier A1 does not supply, at the read node, a current that is added to the current supplied by the first active branch. Amplifier A1 of Perner simply supplies a gate control voltage that drives the gate of transistor Q1 to stabilize voltage Vs′ at the read node 70 at the vicinity of Vs.

Moreover, voltage Vs′ at the read node 70 of Perner, although substantially stable thanks to transistor Q1, is not representative of the conductivity state of the memory cell since it is regulated around Vs whatever the conductivity state of the memory cell is. In an embodiment of the applicant's invention, in contrast, the voltage representative of the conductivity state of the memory is not the read voltage but the VMID1 voltage that drives the input of the inverting gate INV.

Thus, if we consider that in Perner the voltage representative of the conductivity state of the memory is the gate control voltage output by operational amplifier A1, it would be wrong to assert that this voltage remains substantially stable upon a current draw at the read node. On contrary, this voltage is a feedback signal that follows all the variations of the current at the read node 70 so as to maintain the read voltage Vs′ at the vicinity of Vs.

Therefore, neither the sense side (left side) nor the reference side (right side) of the sense amplifier of Perner contains the applicants' disclsoed second active branch. Therefore, the Examiner has not proved that Perner's sense amplifier discloses the applicant's second active branch.

III. Discussion of the Claims

Independent claim 1 recites that the first active branch comprises a means for supplying a read current at the read node. As explained above, this feature is not disclosed, taught, or suggested by Perner. Perner's sense amplifier only comprises the pull-down transistor Q1 that controls a voltage at the read node 70, and does not supply the recited read current at the read node. Accordingly, independent claim 1 is allowable over Perner on the basis of this feature.

Independent claim 1 is further allowable over Perner because it recites that the second active branch comprises a means for supplying a current that is added to the current supplied by the first active branch at the read node. As explained above, this feature is also not disclosed, taught, or suggested by Perner. Perner does not have any sort of second active branch that supplies the current that is added to the current supplied by the first active branch at the read node as recited in claim 1.

Accordingly, claim 1 is allowable over Perner. Some minor amendments have been made to claim 1 to provide proper antecedent basis and to make some other relatively minor changes.

Independent claim 18 currently recites a first branch that provides a first read current to the read node. As explained above, this feature is not disclosed, taught, or suggested by Perner.

Independent claim 18 further recites that the second active branch provides a second current to the read node. As explained above, this feature is not found in Perner, since Perner does not provide a second branch that provides a current to the read node as recited in claim 18. Accordingly, claim 18 is allowable over Perner.

Claim 18 is amended to make some corrections to the recited language. More specifically, the term "branch" was erroneously not included in two locations in the claim.

New dependent claims 19 and 20 are added. Dependent claim 19 recites that the first and second currents are added such that a voltage at the data sense node representative of a conductivity state of the memory cell remains substantially stable upon current draw at the read

node. This feature is not disclosed, taught, or suggested by Perner, as explained above. Accordingly, new claim 19 is allowable.

New claim 20 recites a pair of transistors at each of the first and second branches to respectively provide a first and second current. Perner does not disclose, teach, or suggest such an architecture. For instance, Perner does not disclose a first branch that provides the first current, and a second branch that provides the second current. Accordingly, new claim 20 is allowable over Perner.

IV. Conclusion

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Thus, given the above amendments and accompanying remarks, the independent claims are now in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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